Remarks

Applicant respectfully requests reconsideration of this application as amended. No claims have been amended. No claims have been cancelled. Therefore, claims 1-33 are presented for examination.

Claims 1-3, 8, 10, 14-17, 21, 23-25, and 31-33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi et al. (U.S. Patent No. 5,652,857), Corcoran et al. (U.S. Patent No. 6,449,689), and Kim et al. (U.S. Patent No. 6,859,870). Applicant submits that the present claims are patentable over any combination of Shimoi, Corcoran and Kim.

Shimoi discloses a disk control apparatus for recording and reproducing compression data to physical device of direct access type. The apparatus includes a cache memory between a host computer and a disk drive. The cache memory is divided into a non-compression cache memory for storing non-compression data on a logic block unit basis and a compression cache memory for storing compression data on a compression group unit basis having the same size as that of the logic sector of the disk drive. A compressing circuit extracts the data stored in the non-compression cache memory on a logic block unit basis and compresses the data. A compression group forming unit collects the compression data of the logic block unit by the compressing circuit unit, thereby forming a compression group and storing the compression group into the compression cache memory. An expanding circuit unit extracts the data stored in the compression cache memory on a compression group unit basis, expands, and develops into the non-compression cache memory. See Shimoi at col. 3, ll. 23-65.

Corcoran discloses a system and method for organizing compressed data on a storage disk to increase storage density. The method and system include a compressor for

compressing a data block into a compressed data block, wherein N represents a compression ratio. The storage disk includes a first storage partition having N slots for storing compressed data, and a second storage partition also having N slots for storing overflow data. Each of the N slots in the first partition includes at least one address pointer for pointing to locations in the second partition. According to a further aspect of the system and method, if the compressed data block is less than or equal to 1/N of the data block size, then the compressed data block is stored in a first slot in the first storage partition. If the compressed data block is greater than 1/N of the data block size, then the first 1/N of the compressed data block is stored in the first slot in the first storage partition and a remainder of the compressed block is stored in one or more slots in the second storage partition. The address pointer in the first slot is then updated to point to the one or more slots in the second storage partition. See Corcoran at Abstract.

Kim discloses an instruction being stored in main memory in an uncompressed format and being compressed before being stored in a cache memory. See Kim at col. 1, ll. 61-67.

Claim 1 of the present application recites a cache controller having compression logic to determine that a retrieved cache line is to be combined with a resident companion cache line to form the compressed cache line if the companion cache line is resident in the cache memory and to store the compressed cache line in the cache line of the resident companion. Applicant submits that Shimoi, Corcoran and Kim all fail to disclose or suggest a process of *determining that a retrieved cache line is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory.*

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Kim has been cited as disclosing such a feature. However, Kim merely discloses an embodiment where an instruction is compressed prior to being stored in a cache. There is no disclosure, or reasonable suggestion in Kim of *determining that a retrieved cache line is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory.*

Since Shimoi, Corcoran and Kim all fail to disclose or suggest determining that a retrieved cache line is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory and storing the compressed cache line in the cache line of the resident companion, any combination of Shimoi, Corcoran and Kim would also fail to disclose or suggest such features. Therefore claim 1, and its dependent claims, is patentable over the combination of Shimoi, Corcoran and Kim since none of the references disclose or suggest processes.

Independent claims 15, 24 and 31 include limitations similar to those recited in claim 1. Thus, claims 15, 24 and 31, and their respective dependent claims, are patentable over the combination of Shimoi, Corcoran and Kim for the reasons stated above with respect to claim 1.

Claims 4-7, 9, 18-20, 22, and 26-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi, Corcoran, and Kim, and further in view of Obara (U.S. Patent No. 6,115,787). Applicant submits that the present claims are patentable over any combination of Shimoi, Corcoran, Kim and Obara.

Obara discloses storing compressed records into a cache memory of a disk storage system in an easy-to-read manner. Data to be stored in the cache memory is divided into plural data blocks each having two cache blocks in association with track blocks to which the

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data belongs and are compressed. The respective data blocks after the compression are stored in one or plural cache blocks. Information for retrieving each cache block from an in-track address for the data block is stored as part of retrieval information for the cache memory. When the respective data blocks in a record is read, the cache block storing the compressed data block is determined based on the in-track address of the data block and the retrieval information. See Obara at Abstract.

Nevertheless, Obara does not disclose or suggest determining that a retrieved cache line is to be combined with a resident companion cache line to form a compressed cache line if the companion cache line is resident in the cache memory and storing the compressed cache line in the cache line of the resident companion. As discussed above, Shimoi, Corcoran and Kim all fail to disclose or suggest such features. Therefore, any combination of Shimoi, Corcoran, Kim and Obara would also not disclose or suggest the features. As a result, the present claims are patentable over the combination of Shimoi, Corcoran, Kim and Obara.

Claims 11-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi et al., Corcoran et al., and Kim et al., as applied to claim 10 above, and further in view of Cypher (U.S. Patent No. 6,629,205). Applicant submits that the present claims are patentable over any combination of Shimoi, Corcoran, Kim and Cypher.

Cypher discloses a cache memory including a plurality of memory chips that are configured to collectively store a plurality of cache lines. Each cache line includes data and an associated cache tag. The cache tag may include an address tag which identifies the line as well as state information indicating the coherency state for the line. Each cache line is stored across the memory chips in a row formed by corresponding entries (i.e., entries

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accessed using the same index address). The plurality of cache lines is grouped into separate

subsets based on index addresses, thereby forming several separate classes of cache lines.

The cache tags associated with cache lines of different classes are stored in different memory

chips. During operation, the cache controller may receive multiple snoop requests

corresponding to, for example, transactions initiated by various processors. The cache

controller is configured to concurrently access the cache tags of multiple lines in response to

the snoop requests if the lines correspond to differing classes. See Cypher at Abstract.

However, Cypher does not disclose or suggest determining that a retrieved cache line

is to be combined with a resident companion cache line to form a compressed cache line if

the companion cache line is resident in the cache memory and storing the compressed cache

line in the cache line of the resident companion. As discussed above, Shimoi, Corcoran and

Kim fail to disclose or suggest such limitations. Therefore, any combination of Shimoi,

Corcoran, Kim and Cypher would also not disclose or suggest the limitations. Accordingly,

the present claims are patentable over the combination of Shimoi, Corcoran, Kim and

Cypher.

Applicant submits that the rejections have been overcome and that the claims are in

condition for allowance. Accordingly, applicant respectfully requests the rejections be
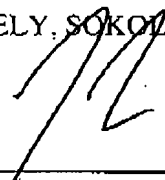
withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains

any issue with allowance of the case.

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Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: <u>November 7, 2007</u>

Mark L. Watson
Reg. No. 46,322

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(303) 740-1980

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